An advanced FACTS controller for power flow management in transmission system using IPFC

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Abstract— **This paper presents an advanced FACTS controller for power flow management in transmission system using IPFC. Regulator uncertainty, cost, and lengthy delays to transmission line construction are just a few of the barriers that have resulted in the serious deficiency in power transmission capacity that currently prevails in many regions. Solving these issues requires innovative tool on the part of all involved. Low environmental-impact technologies such as flexible AC transmission system (FACTS) and dc links are a proven solution to rapidly enhancing reliability and upgrading transmission capacity on a long-term and cost-effective basis. Interline power flow controller (IPFC) is a new concept of FACTS controller for series compensation with the unique capability of power flow management among multi-line of a substation. In this work mainly concentrated on choosing a suitable voltage source converter, to employ it in the IPFC. A 48 pulse multilevel inverter has been developed by cascading several units of three level diode clamped multilevel inverter (NPCI) with the help of phase shifting transformer. A simple and typical test system model has been developed to check the performance of IPFC an advanced FACTS controller. A closed loop controller has been developed to maintain the voltage profile of the test system.**

Keywords- FACTS controllers, IPFC, Multilevel inverter, NPCI, VSC

I. INTRODUCTION

Deregulated electric power industries have changed the way of operation, structure, ownership and management of the utilities. The existing power transmission networks may not have been able to accommodate all the new scenarios for electricity trades. The energy transaction in open access environment may lead to unexpected amount and direction of power flow through some transmission corridors, resulting in the need for some load to be dropped momentarily in order to maintain the system security. It is further endangered by relative decline in transmission expansion due to requirement of huge investment coupled with the problems in acquiring right of- way for the new transmission facilities and the concerns towards environment and cost. It may not be ideal for the power generation company to drop some loads, which may cost them penalties while the system operates near its operating limits in terms of security. Curtailment of loads under contract, costs the power companies, a reduction in their regular tariffs. It is always preferable to have minimum curtailment in the system at all as it is better for the system reliability and fulfilling the contractual obligations; therefore,

load curtailment reduction is an important issue to be addressed in electricity markets.

With increasing demand and supply in the power systems, maintaining the security, stability and reliability have become a challenging task, specifically in the emerging electricity market scenario [1]. The basic challenge in the evolving deregulated power system is to provide a transmission network capable of delivering contracted power from suppliers to consumers over large geographic area under market forces-controlled, and continuously varying patterns of demand and supply. Flexible AC Transmission Systems (FACTS) are being popularly used by utilities due to their capability to enhance power system static as well as dynamic performance.

The FACTS controllers utilize power electronics based technology and can provide dynamic control on line power flows, bus voltages and thus enhance system stability and security. These capabilities allow transmission system owners and operators to maximize asset utilization and effectively execute additional bulk power transfers. The FACTS controllers have been broadly developed on two different principles, one that alters the line series reactance or bus shunt reactance or voltage phase difference across a line and utilizes conventional thyristor 2 switches for control. These include static VAR compensator (SVC), Thyristor Controlled Series Compensator (TCSC) and Thyristor Controlled Phase Angled Regulator (TCPAR). The second that controls the series injected voltage and/or shunt injected current employing voltage source converters include Static Synchronous Compensator (STATCOM), Static Synchronous Series Compensator (SSSC) and Unified Power Flow Controller (UPFC). The SVC and STATCOM are the shunt compensators, whereas, TCSC and SSSC are the series compensators. [1] The UPFC combines both series and shunt compensators, and offers more versatile characteristics.

II. INTERLINE POWER FLOW CONTROLLER

A. Introduction

The IPFC, proposed by Gyugyi with Sen and Schauder addresses the problem of compensating a number of

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transmission lines at a given substation. The IPFC scheme, together with independently controllable reactive series compensation of each individual line, provides a capability to directly transfer real power between the compensated lines [1]. This capability makes it possible to equalize: both real and reactive power flow between the lines reduce the burden of overload line by real power transfer; compensate against resistive line voltage drops and the corresponding reactive power demand; and increase the effectiveness of the overall compensating system for dynamic disturbances.

B. Configuration Of Interline Power Flow Controller

It is common that, the IPFC employs a number of dc to ac inverters in order to offer series compensation for each line. As a new concept for the compensation and effective power flow management, it addresses the target of compensating a number of transmission lines at a given substation. The IPFC is a combination of two or more independently controllable SSSC which are solid-state voltage source converters. As shown in Fig. 1, the unit 1 of IPFC can be operated as SSSC.

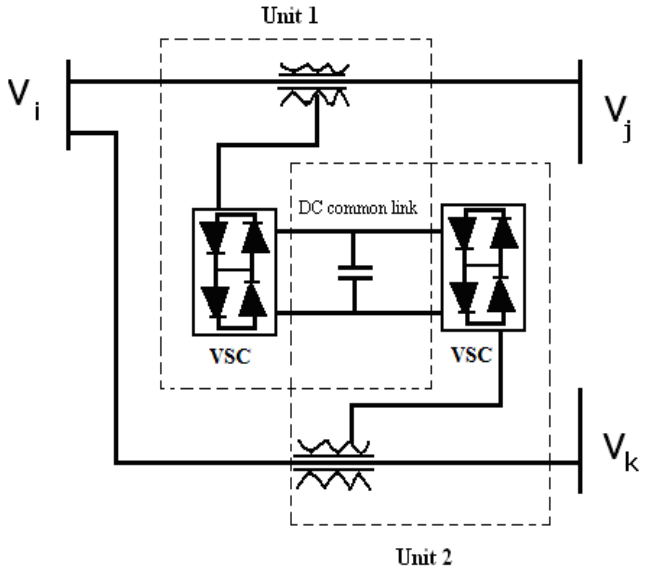

Figure 1. Basic Configuration Of Interline Power Flow Controller

Conventionally, series capacitive compensation fixed, thyristor controlled or SSSC based, is employed to increase the transmittable real power over a given line and to balance the loading of a normally encountered multi-line transmission system. They are controlled to provide a capability to directly transfer independent real power between the compensated lines while maintaining the desired distribution of reactive flow among the line [2] and [3].

C. Basic principle of interline power flow controller

The simplified schematic of IPFC model is shown in Fig.2.1, with this scheme an addition to provide series reactive compensation, any converter can be controlled to supply real power to the common dc link from its own transmission line. Thus an overall surplus power can be made from the underutilized lines which then can be used by other lines for real power compensation. In this way some of the converters, compensating overloaded lines or lines with heavy burden of reactive power flow, can be equipped with full two dimensional, reactive and real power control capability, similar to that offered by the UPFC. Evidently, this arrangement mandates the rigorous maintenance of the overall power balance at the common dc terminal by appropriate control action, using the general principle that the overloaded lines are to provide help in the form of appropriate real power transfer, for the overloaded lines.

The IPFC is designed with a combination of the series connected VSC which can inject a voltage with controllable magnitude and phase angle at the fundamental frequency while DC link voltage can be maintained at a desired level. The common dc link is represented by a bidirectional link (P12 =P1pq = -P2pq) for real power exchange between voltage sources is shown in the Fig. 2.

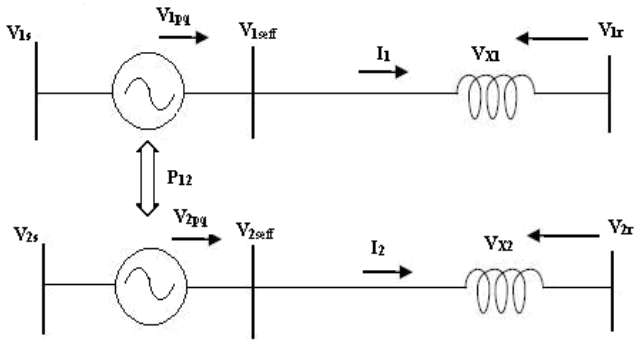

Figure 2. Two-Inverter Interline Power Flow Controller

Transmission line1, represented by reactance X1, has a sending-end bus with voltage phasor V1s and a receiving –end voltage phasor V1r. The sending –end voltage phasor of Line2, represented by reactance X2, is V2s and the receiving-end voltage phasor is V2r. Simply, all the sending-end and receiving-end voltages are assumed to be constant with fixed amplitudes, V1s = V1r = V2s = V2r =1 p.u., and with fixed angles resulting in identical transmission angle s1 = s2 for the two systems. The two line impedances, and the rating of the two compensating voltage sources, are also assumed to be identical. This means V1pqmax = V2pqmax and X1 = X2. Although in practice system1 and system 2 could be likely different due to different transmission line voltage, impedance and angle [4].

We assumed system1 is arbitrarily selected to be the prime system for which free controllability of both real and reactive line power flow is stipulated to derive the constraints the free controllability of system1 forces on the power flow control of system 2. A phasor diagram of system1 illustrated in Fig. 3 defines the relationship between V1s, V1r, Vx1 (the voltage phasor across X1) and the inserted voltage phasor V1pq, with controllable magnitude and angle. V1pq is added to the sending-end voltage V1seff = V1s + V1pq. So V1seff – V1r, the difference sets the compensated voltage phasor or Vx1 across reactance X1. As system1 is varied over its full 360 degree range, the end of phasor V1pq moves along a circle with its center located at

the end of phasor V1s. The area within this circle defines the operating range of phasor V1pq.

So line1 can be compensated. The rotation with angle1of phasor V1pq modulates both the magnitude and the angle of phasor Vx1 and, therefore, both the transmitted real power P1r, and the reactive power Q1r, vary with 1 [5]. This process requires the voltage source representing Inverter1 (V1pq) to supply and absorb both reactive Q1pq and real P1pq power.

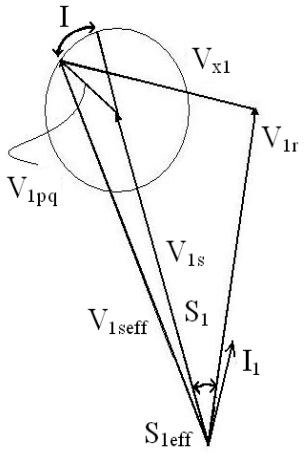

Figure 3. Phasor diagram of system 1

III. VOLTAGE SOURCE CONVERTER

A. *Neutral point clamped multilevel inverter*

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level.

The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. The three phase three level diode clamped multilevel inverter is shown in Fig.4.

Normally an n-level diode-clamped multilevel inverter has 2(n-1) main switches (SW1-SW4,) and 2(n-1) main diodes (D1-D8). The three level NPC-VSC features two additional diodes per phase leg as compared to a two level VSC with a direct series connection of two devices per switch position. These so-called NPC diodes link the midpoint of the "indirect series connection" of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point N and enables the three-level characteristic of the topology.

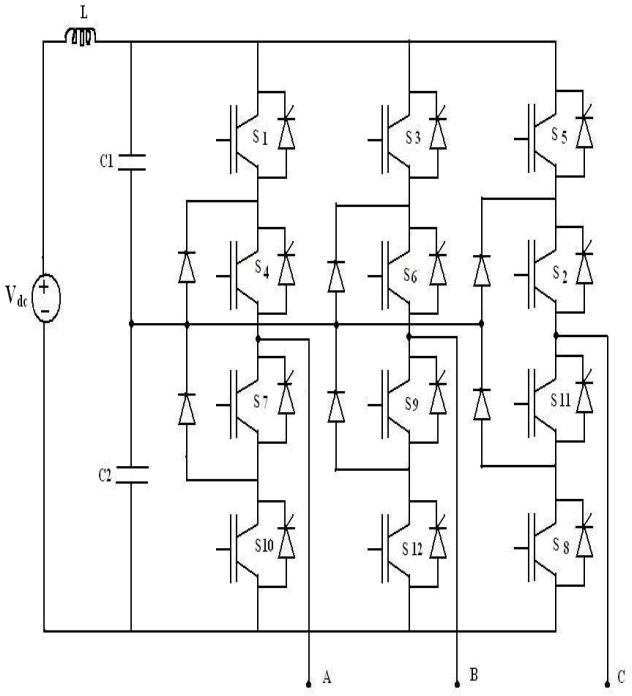

Figure 4. Three level diode clamped inverter

B. *Multilevel inverter control technique*

The fundamental requirement for the diode-clamped multilevel inverter switching scheme is to ensure that the switches operate in the contiguous modes listed in Table I. The most popular and simple methods are step modulation and sinusoidal pulse width modulation (SPWM). In this work SPWM switching strategy [6] is employed. In SPWM technology, two carrier signals are compared with the sinusoidal reference waveform the result is used to control all the main switches.

TABLE I SWITCHING STATES FOR PHASE A

Condition	Switch states for Phase A		State
	ON	OFF	
$V_r > (V_{t1}, V_{t2})$	S_1 S_4	S_7 S_{10}	$+V_{dc}/2$
$V_{t1} > V_r > V_{t2}$	S_4 S_7	S_1 S_{10}	0
$V_r < (V_{t1}, V_{t2})$	S_7 S_{10}	S_1 S_4	$-V_{dc}/2$

C. *48 Pulse multilevel inverter*

48-pulse inverters are obtained by combining four twelve pulse VSIs with an adequate phase shifts between them. Each of the VSI needs a coupling transformer of which two of them require a star- star transformer with a turns ratio of 1:1 and the remaining two require a delta – star with a turns ratio of 1:√3. The output of the phase shifting transformers is connected in series to cancel out the lower order harmonics. The 48-pulse inverter topology is shown in the Fig. 5.

To create a 48 pulse waveform with a harmonic content in the order of m=48r ±1, (where r = 0, 1, 2….) the four

twelve pulse converter voltages need to be phase shifted. This is implemented by introducing appropriate phase shift in the phase shifting transformer and the gate pulse pattern of individual VSI. Table II shows the phase displacements applied to the gate pulse pattern of each VSI and the corresponding phase shifting transformer.

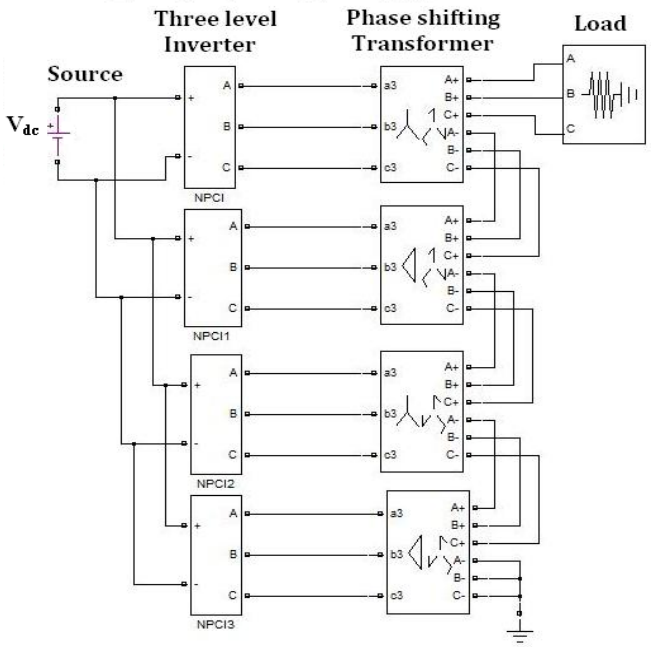

Figure 5. 48-Pulse inverter topology

TABLE II PHASE DISPLACEMENT FOR A 48- PULSE VSI

Coupling transformer	Gate pulse pattern	Phase shifting transformer
Star - Star	-7.5°	-7.5°
Delta - Star	-37.5°	-7.5°
Star - Star	7.5°	7.5°
Delta - star	-22.5°	7.5°

So far 48 pulse inverter is developed using eight phase shifting transformer [7]. In the proposed inverter configuration only four phase shifting transformers are employed. From the cost perspective view it is a great advantage. This 48 pulse inverter is involved as VSC.

IV. SIMPLE POWER TRANSMISSION SYSTEM MODEL

A. Power system model with VSC

In the open loop system, two transmission lines has been taken and the VSC's are coupled in to the transmission system with the help of series insertion transformer. The sources of the VSC's are connected by means of a common DC link capacitor. This configuration gives the IPFC model.

The power system model has been generated in the matlab simulation tool to check the performance of the interline power flow controller. The power system specification has been set as, 230 kV generating station, transmission line of length 100 km with 50 Hz frequency, step down transformer with primary as 230 kV and secondary as 33kV, and PQ load of active power 500kW and inductive reactive power is variable has been designed.

B. Power system model with closed loop controller for IPFC

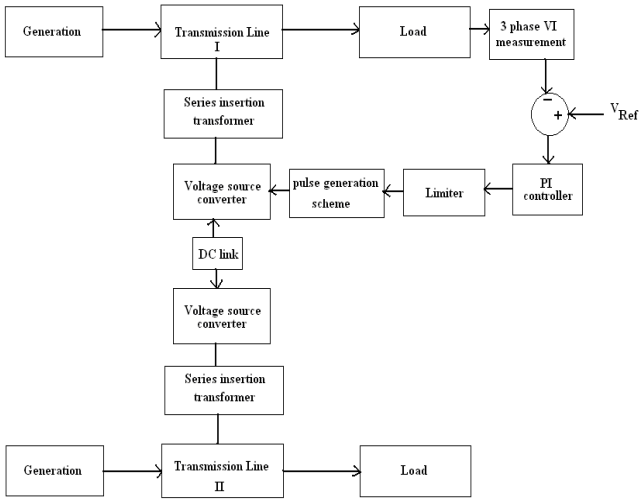

Figure 6. Closed loop system

The voltage is maintained with the help of PI controller. The measurement block gives the load voltage in kV that has been fed in to the comparator where it has been compared with the reference value which has been set initially. The error value has been sent to the PI controller. And the result is limited by the saturation block and then it has been multiplied to produce the signal. The signal thus obtained is the reference wave in pulse generation scheme of the VSC's. The voltage has been regulated with the help of this reference wave; the pulse has been generated accordingly.

V. SIMULATION RESULTS

A. Three level diode clamped multilevel inverter

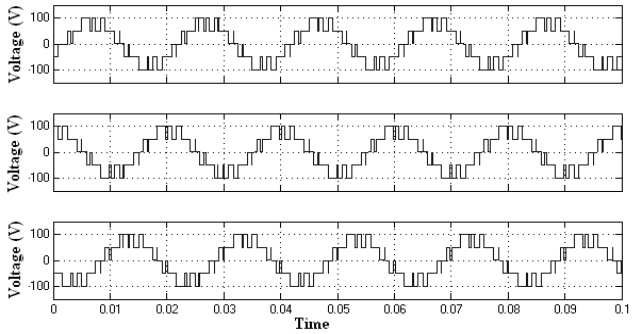

Figure 7. Line to neutral voltages

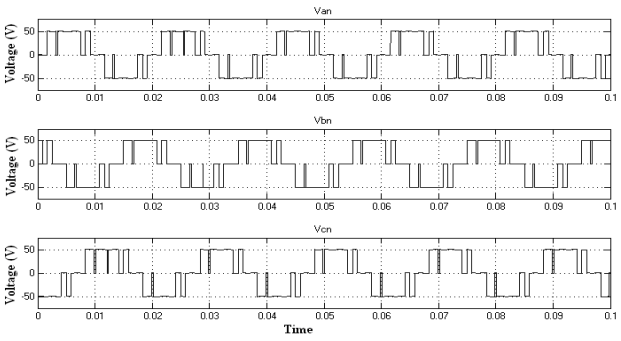

Figure 8. Phase to phase voltages

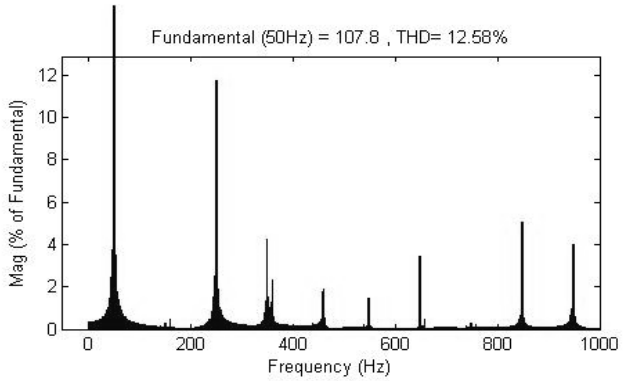

Figure 9. Total harmonic distortions

B. *48 pulse mulitilevel inverter*

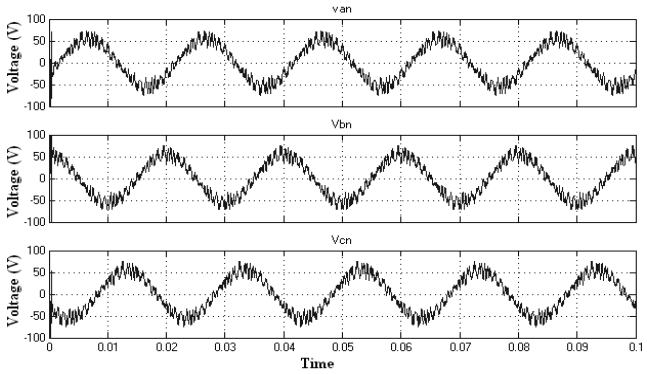

Figure 10. Line to neutral voltages

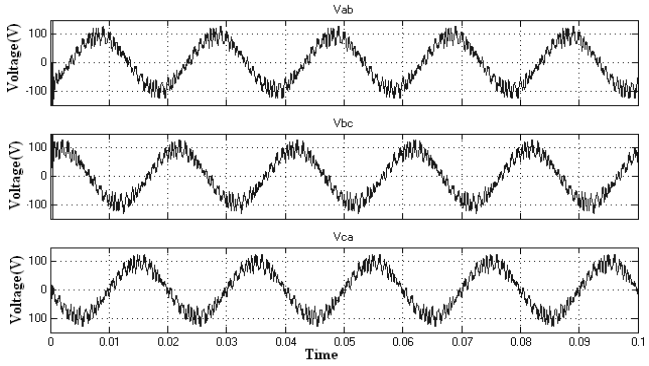

Figure 11. Phase to phase voltages

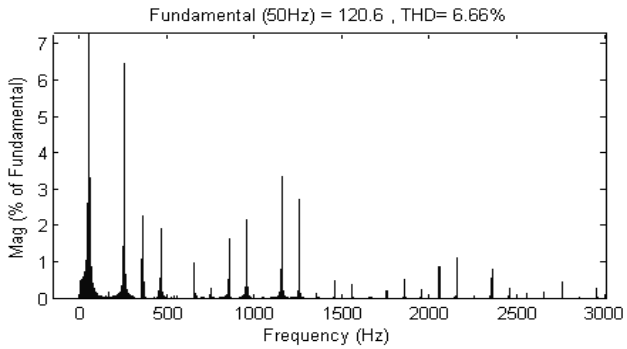

Figure 12 Total harmonic distortions

C. *Interline power flow controller*

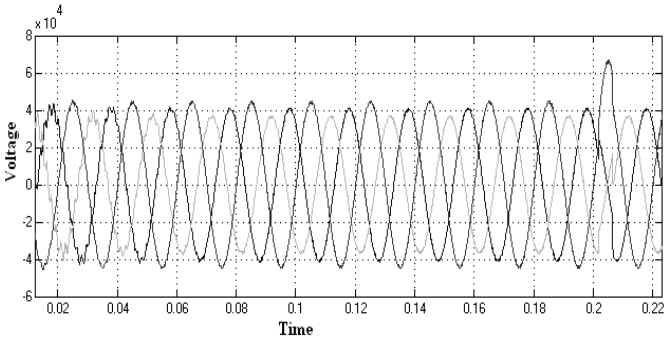

Figure 13 Load voltage

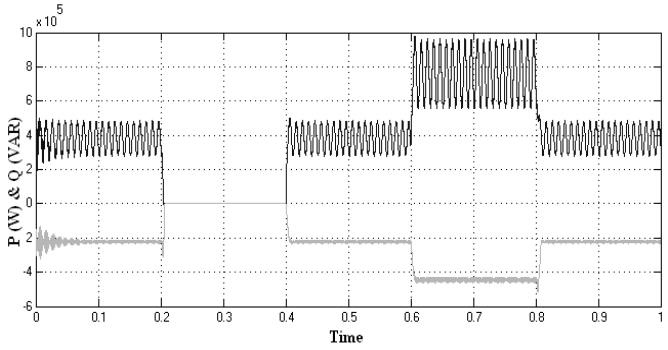

Figure 14 Real and reactive power of the transmission system

D. *IPFC with PI controller*

Load voltage:

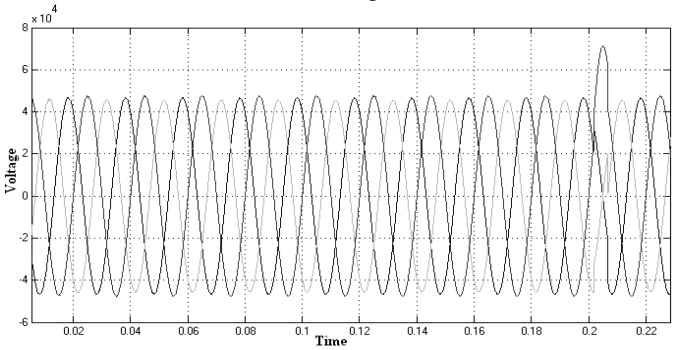

Figure 15 Load voltage

Voltage profile has been maintained throughout the transmission system.

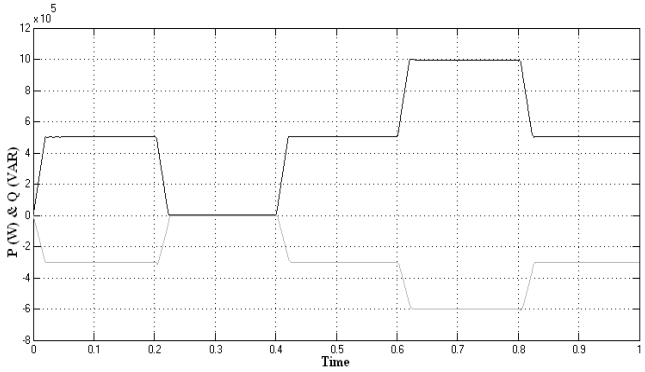

Figure 16 Real and reactive power of the transmission system

The result comparison between the power system with IPFC and closed loop control of the power system with IPFC configuration for load variation is given in the table III.

TABLE III RESULT COMPARISONS BETWEEN OPEN LOOP AND CLOSED LOOP POWER SYSTEM WITH IPFC

S. No	Inductive reactive power (KVAR)	Real power (kW)		Reactive power (KVAR)		Load voltage (kV)	
		Open loop	Closed loop	Open loop	Closed loop	Open loop	Closed loop
1	100	386.8	5.023	741.8	996.2	25.8	33.61
2	200	387.3	5.023	148.3	199.2	28.8	32.92
3	300	388.5	5.023	222.4	298.8	25.3	33.02
4	400	389.3	5.023	296.4	398.4	31.3	33.68
5	500	390.9	5.023	370.5	497.9	28.4	32.97

VI. CONCLUSION

VSC considered is a 48 pulse multilevel inverter. The proposed 48 pulse inverter has been simulated. It is observed from the simulated result that it is almost sinusoidal with very less THD. This inverter configuration is employed to realize the IPFC. Typical and simple power system model has been proposed to investigate the performance of the IPFC, composed of 48 pulse inverter. It has been found that the IPFC injects the series voltage of controllable magnitude and phase angle in order to maintain the real and reactive power flow over the transmission line. Closed loop controller has been developed for the IPFC configuration to maintain the voltage profile at any instant of the power system. The simulation results show the improved transfer capability in the transmission system.

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